IN THE CLAIMS

Please amend claim 31 as follows. All claims have been provided as a courtesy to the Examiner.

1　31.　(Twice Amended)　A memory device, comprising:

2　　a memory array;

3　　a register to store at least one bit indicating a suspend status of a write operation

4　for the memory array; and

5　　a control circuit coupled to said memory array and said register, said control

6　circuit to update said register and to control the output of a status signal representing said

7　protection status of a [said] data modification operation, and wherein said control circuit

8　includes:

9　　　a first state machine to receive commands for accessing said memory

10　　array or said register [update at least one of said bits indicating said suspend

11　　status of said write operation in response to a suspend signal], and

12　　　a second state machine coupled to said first state machine and to execute

13　　the commands received by said first state machine [control the output of said

14　　status signal in response to a status request signal].

1　32.　(Unchanged)　The memory device of claim 31, wherein said write operation

2　represents a byte write operation.

1　33.　(Unchanged)　The memory device of claim 31, wherein said suspend signal

2　represents a byte write suspend command.

--2--

1 34. (Unchanged) The memory device of claim 31, wherein said control circuit is to

2 receive a status request signal and said register is to output said status signal in response

3 to said status request signal, said status signal having a first state to indicate said write

4 operation is suspended and a second state to indicate said write operation is not

5 suspended.

1 35. (Unchanged) The memory device of claim 35, further comprising:

2   at least one data input/output coupled to said control circuit, wherein the at least

3 one data input/output is to receive said status request signal from a processor and to

4 provide said status signal to said processor.

1 36. (Unchanged) The memory device of claim 31, further comprising:

2   a status output coupled to said register, wherein said status output is to provide a

3 second status signal if said status output is polled, and wherein said second status signal

4 having a first state to indicate said write operation is suspended and a second state to

5 indicate said write operation is not suspended.

1 37. (Unchanged) The memory device of claim 31, wherein said status request signal

2 is a read status register command.